**Dr. VAIBHAV NEEMA**
Assistant Professor (Sr. Grade), Electronics & Telecommunication Engineering Department
Institute of Engineering and Technology, Devi Ahilya University, Indore.
(NAAC "A" Grade)

**Educational Background:**

| Qualifications | Institute/University/ College/Board | Year | %Age |
|---|---|---|---|
| **Doctoral in Philosophy** (Ph. D.) Titled "Evolution and Evaluation of Low power design technique for Nanoscale CMOS Circuit" | Institute of Engineering and Technology, Devi Ahilya University, Indore, India | 14th Feb, 2012 | - |
| Master of Technology (M. Tech.) (Microelectronics) (3 Semester PG Course) | University Center of Instrumentation and Microelectronics (UCIM), Panjab University, Chandigarh, India | 2003 | 69.00 % |

- Expert Lecture in the three days Summer Course in the area of Internet of Things (IoT) organized by **Aalto University, Electrical Engineering Department, Finland** for Session June 2017.
- **Research Project:**

**(a) Ongoing Funded Projects:**

1) Entitled: Aalto- IIT-I cooperation for the skill developments of IoT-based implementation

| | |
|---|---|
| Funding Agency | Finnish Ministry of Education and Culture<br>CIMO* Asia programme 2016 |
| *(*international mobility and co-operation- -As an agency of the Finnish Ministry of Education and Culture)* | |
| Coordinator | Dr Vaibhav Neema from IET-DAVV, Indore |
| Consortium Members | From Finland: Aalto University School of Electrical Engineering, Finland<br>From India: IIT Rookee, IIIT Hyderabad, NIT Jalandhar, |
| Funding Amount | Euro 50,000/- |
| Project Number | Intia-1-2016-3 |
| Starting Date | Sep 2016 |
| Duration | 02 Year |

2) Entitled: Design and Implementation of Leakage Reduction Technique for High Speed Nanoscale CMOS Circuit:

| | |
|---|---|
| Funding Agency | M.P. Council of Science & Technology, Bhopal |
| Principal Investigator | Dr Vaibhav Neema |
| Co-Investigator | NIL |
| Funding Amount | Rs. 8,01,250/- |

| | |
|---|---|
| Endt No | 1950/CST/R&D/Phy& Engg Sc/2015 |
| Starting Date | August, 27th 2015 |
| Duration | 02 Years |

3) Entitled: Development of High stable, Low Leakage, High Speed SRAM Cell:

| | |
|---|---|
| Funding Agency | University Grant Commission (UGC), Under Seed Money project scheme. |
| Principal Investigator | Dr Vaibhav Neema |
| Co-Investigator | NIL |
| Funding Amount | Rs. 1,00,000/- |
| Endt No | Dev-III/Seed money/proposal/2014/679 |
| Starting Date | May, 8th 2014 |
| Duration | 01 ear (Extended for 1 Year) |

**(b) Grants Received:**

Travel grant : for session chair and present research paper in International Conference on Electronics Devices, Systems & Application at University Technology of MARA, Malaysia.

| | |
|---|---|
| Funding Agency | M.P Council of Science & Technology, Bhopal |
| | Dr Vaibhav Neema |
| Funding Amount | Rs. 30,000/- |
| Endt No | CST/TG/2010-11 |
| Starting Date | April, 6th 2010 |

- **Submitted Research Projects:**

1) Entitled: Development of Power Reduction Technique for Battery Operated Nanoscale CMOS circuit

| | |
|---|---|
| Funding Agency | Major Research Proposal (MRP) under 12th plan of University Grant Commission (UGC), New Delhi |
| Principal Investigator | Dr Vaibhav Neema |
| Co-Investigator | NIL |
| Funding Amount | Rs. 20,20,000/- |
| Endt No | MRP-MAJOR-ELEC-2014-51262 |
| Starting Date | - |
| Duration | 03 Year |

2) Entitled: Novel Circuit approach for Low power battery operated System Design.

| | |
|---|---|
| Funding Agency | AICTE – Research Promotional Scheme 2016-17 |
| Principal Investigator | Dr Vaibhav Neema |
| Co-Investigator | NIL |
| Funding Amount | Rs. 23,50,000/- |

| | |
|---|---|
| Endt No | AQIS Application Id: 1-3346471426 |
| Starting Date | - |
| Duration | 03 Year |

- **Completed Research Fellowship:**
  Title of Project: Verification of VLSI Subthreshold Leakage Reduction Technique "VSECURE" based cells (INV, NAND2, NOR2 and Single bit Full-Adder) using Cadence EDA tool.

| | | |
|---|---|---|
| Duration | : | 1 Month from 30th May, 2011 |
| Organization | : | Visvesvaraya National Institute of Technology, Nagpur |
| Supervisor | : | Prof (Dr.) Rajendra M Patrikar |

- **Institutional Ongoing Research Project**

1) IoT enabled Green energy based Water Quality monitoring System:

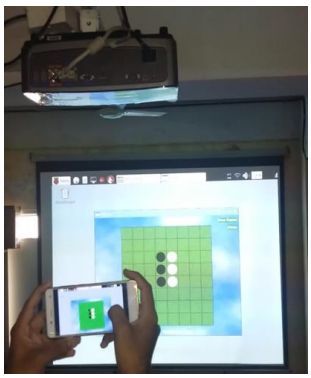
In current scenario, the major focus of system designers is to reduce the size of the system and to make it compact, robust and reliable, to optimize power performance such that device can operate in a low power environment. Keeping this objective in mind, the proposed system has a small size, low cost and high integration wireless SoC, the Esp8266 NodeMCU-12E Wi-Fi module with embedded microcontroller unit. For the sustainable development and deployment of the system it is made to operate on solar energy. The initial phase of system design includes market search of the controller cum Wi-Fi NodeMCU-12E and various sensors employed to monitor water level and water quality. For the proposed system the various parameters being measured are pH level, turbidity, Total Dissolved Solid (TDS), conductivity, heavy metals like arsenic, lead, mercury etc. and temperature of water. As far as system design is considered, the water level sensing and pH value detection is successfully done by interfacing the ultrasonic ranging module HC-SR04 and pH sensor with the NodeMCU-12E. Data acquisition from the sensors and obtaining it on the webpage through Wi-Fi can be accomplished as per the request from user.

**Applications:**

- The system may find its best application in city's municipal water distribution system. It will eliminate the need of labour to track the water level of overhead tanks across the city and can easily replace the present water quality testing procedures.
- It would be a innovative approach to the government's River Cleaning Mission like National Mission for Clean Ganga (NMCG), Narmada cleaning drive etc. The deployment of this system repetitively at a particular distance will let us know that which part of river is being polluted badly and corrective measures would be taken in immediate effect. The level of water in the river can also be known such that water level above the danger can be known and preventive actions can be taken.
- In educational institutions, the system can be used to track the water level and water quality of the tanks and the message regarding the drinkability of water can be displayed.

- The proposed system works on solar power, hence can be implemented in the regions where there is low supply of electricity like in rural areas. As it works on solar energy its deployment in the regions like forests and mountains would let us know about water quality of that regions, because almost all rivers originates from hilly areas and most of the ground water is contributed by the mountains by soaking the rain water.
- Even, the system can be used by the people in household to track the quality of water they are supplied by the water suppliers or water from the tube wells.
- The system can be used by the farmers to track the quality of irrigation water so that high yield of crops can be attained. Knowing the amount of various parameters in water will let him know that which crop will be best suitable for the particular quality of water.

2) Smart Projector using Internet of Things:



Traditional projectors are based on wired connections all over from the CPU to the projector placed at center of the room. Dealing with wires is itself a huge hurdle. The solution to this problem is a wireless projector that can be controlled through smartphones. In smart systems there is a need of avoiding gigantic network of wires and requiring simpler approach. This situation can be handled by developing such a scenario where there is a minimal use of wires in operating and controlling the projector screen. The data to be displayed on the projector is controlled through smartphones rather than using laptops or desktop. This ensures portability.

➢ **Professional Experience (Total 12 Years of Teaching):**

- ✓ 15-Sep, 2007 – till date: Lecturer, Department of Electronics and Telecommunication Engineering, Institute of Engineering and Technology (IET), Devi Ahilya University, Indore (MP), India.
- ✓ 8-Dec, 2006 – 14-Sep, 2007: Lab Engineer Electronics and Instrumentation Engineering Department, Under SMDP VLSI Project Phase II (Government of India funded Project), Shri S.G. Institute of Technology and Science, (SGSITS) Indore (MP), India.
- ✓ 5-July,2005 – 7-Dec,2006:Lecturer, Electronics and Communication Engineering Department, Faculty of Engineering & Technology, Mody Institute of Technology and Science (DEEMED UNIVERSITY) Lakshmangarh (Sikar) Rajasthan ,India
- ✓ Feb, 2003 –4-July, 2005: Lecturer, Electronics and Communication Engineering Department, College of Engineering Roorkee (COER), Roorkee (UA), India.

➢ **Patent: Submitted**

[1]. Dr. Vaibhav Neema, Mr. Praveen Singh, Mr. Nikhil Sharma, Mr. Somendra Singh Rajpoot,Mr. Lavish Patidar , “Wireless Projection for Smart Education using Internet of Things” Through National Research Development Corporation

**Objective:** The main objective of this report is to determine the novelty of the current invention. The other objective of the study is to find the relevant prior art that is directly or in combination of multiple references, overlapping the current significant features present in the invention.

- **Publications:**

**(i) Book Chapter:**

[1]. Shani Jain, Vaibhav Neema, Praveen Singh, Ambika Prasad Shah, "Effect of Process, Voltage and Temperature Variation in DYNOC Approach for Domino Logic Circuits (Chapter 19)", Springer Book Communications in Computer and Information Science Volume 628, 2016, p.p.831-839.
ISBN: 9789811034329 (Print) 9789811034336 (Online)

**(ii) Journals:**
**Submitted Research Papers:**

[1]. Mansimran Kaur, Vaibhav Neema, Deepika Gupta, Santosh Kumar Vishvakarma, "Improvement in Electrical Characteristics of BE-SONOS using High-k Dielectrics in Tunneling Barrier " **Accepted** for Publication in IETE Journal of research.
[2]. Neha Gupta, Priyanka Parihar, Vaibhav Neema, "Application of Source Biasing Technique for Energy efficient DECODER circuit design (Memory array application)" **Submitted** for Publication in Journal of Semiconductors.
[3]. Priyanka Parihar, Neha Gupta, Vaibhav Neema and Praveen Singh, "Analysis and comparative study of different ground-gated asymmetric and symmetric SRAM cell architectures", **Submitted** for Publication in Journal of Circuit, Systems, Computers, World Scientific Publication.
[4]. Priyanka Parihar, Vaibhav Neema and Praveen Singh, "Design and analysis of ultra-low power memory architecture with MTCMOS asymmetrical ground-gated 7T SRAM cell", **Submitted** for Publication in ELSEVIER Integration Journal.

**Published Research Papers:**

[1]. Neha Gupta and Vaibhav Neema, "Design and Analysis of DECODER circuit with Source biasing Technique for Memory array application" IEEE TCVLSI Circuit and Systems Letter, vol. 3, Issue 2, June 2017.

[2]. **Ambika Prasad Shah**, Vaibhav Neema, Shreeniwas Daulatabad and Praveen Singh, "Dual threshold voltage and sleep switch dual threshold voltage DOIND approach for leakage reduction in domino logic circuits", **Springer Microsystem Technologies**, June 2017, pp. 1-14 (DOI: 10.1007/s00542-017-3437-2) [Impact Factor: 0.974]

[3]. Nidhi Tiwari, Priyanka Atre, Priyanka Parihar and Vaibhav Neema, "Highly Robust Asymmetrical 9T SRAM with Trimode MTCOS Technique", **Springer Microsystem Technologies**, May 2017, pp. 1-7 DOI: 10.1007/s00542-017-3434-5 [Impact Factor: 0.974]

[4]. Ambika Prasad Shah, Rajat Kumar Jain and Vaibhav Neema, "A Novel Energy Efficient High-Speed 10-Transistor Full Adder Cell Based on Pass Transistor

Logic", Journal of Nanoelectronics and Optoelectronics, Vol. 12, pp. 1-6. (DOI:10.1166/jno.2017.2030) : **UGC File III no 21792**

[5]. Pushpa Raikwal, Vaibhav Neema, Ajay Verma, "New 8T SRAM Circuit with Low Leakage and High Data Stability Idle Mode at 70nm Technology " Oriental Journal Of Computer Science and Technology. (Accepted)

**UGC File II no 28481**

[6]. S. Daulatabad, V. Neema, A.P. Shah, P. Singh, "8-Bit 250-MS/s ADC Based on SAR Architecture with Novel Comparator at 70 nm Technology Node", ELSEVIER Procedia of Computer Science, 79 (2016) iii–vii, P-589.

[7]. P. Singh, V. Neema, S. Daulatabad, A.P. Shah, "Subthreshold Circuit Designing and Implementation of Finite Field Multiplier for Cryptography Application", ELSEVIER Procedia of Computer Science, 79 (2016) iii–vii, P-597.

[8]. Sonal Jain, Vaibhav Neema, Deepika Gupta, and Santosh Kumar Vishvakarma, "Investigation of Band-Gap Engineered Silicon-Oxide-Nitride-Oxide-Silicon Flash Memory with High-k Dielectrics in Tunnel Barrier and Its Impact on Charge Retention Dynamics", Journal of and Optoelectronics Vol. 11, pp. 1–6, 2016. **UGC File III no 21792**

[9]. Sonal Jain, Deepika Gupta, Vaibhav Neema, and Santosh Vishwakarma, "BE-SONOS flash memory along with metal gate and high-k dielectrics in tunnel barrier and its impact on charge retention dynamics", Journal of Semiconductors, Vol. 37, No. 2, February 2016**. UGC File III no 22716**

[10]. Ambika Prasad Shah, Vaibhav Neema and Shreeniwas Daulatabad, "DOIND: A Technique for Leakage reduction in Nanoscale Domino Logic Circuits", Journal of Semiconductors, Vol. 37, No. 2, February 2016: **UGC File III no 22716 2016**

[11]. Pushpa Raikwal, Vaibhav Neema, Ajay Verma "Cluster Based Sleep Transistor Approach for Low Power 6T SRAM Cell" Journal of VLSI Design Tools & Technology ISSN: 2249-474X (online), ISSN: 2321-6492(print) Volume 6, Issue 1

[12]. Pushpa Raikwal, Vaibhav Neema, Ajay Verma, "Performance Analysis of Various Techniques on 6T SRAM Cell", Journal of Circuits and Systems, Vol 3, pp 29-33, 2015. ISSN 2321-7502.

[13]. Deeksha Paliwal , Neeshu Sahu, Shalini Tiwari, Vaibhav Neema, "Power and Delay Analysis for MTCMOS( Leakage Reduction Technique) inverter tree", In International Journal of Science and Innovative Engineering and Technology (IJSIET), May 2015 , ISBN 978-81-904760-7-2

[14]. Manas Gupta and Vaibhav Neema , "Algorithm Implementation for power reduction in MTCMOS Circuits", Journal of Basic and Applied Engineering Research (JBAER)., Dec 2014 , ISSN-2350-0077, pp18-20.

[15]. Vaibhav Neema, Ruchi Jain , Akrati Singh, Neeta Nihale , "Dynamic and Static Analysis of Different Full Adder Topology at 180nm Technology Node", IJCA Proceedings on International Conference and Workshop on Emerging Trends in Technology 2013 ICWET(3):1-4, April 2013. Published by Foundation of Computer Science, New York, USA.(ISSN 0975-8887)

[16]. Vaibhav Neema, Pratibha gupta, "design strategy for barrel shifter using Mux at 180nm Technology node" IJISME 2013 , July 2013 , volume 1 issue 8. (ISSN : 2319-6386) [9]

[17]. Vaibhav Neema, Priyanka Pawar,"Design tradeoff Analysis and implementation of Digital Binary Adders using Verilog, IJSR, Aug 2013 , Vol 3 Issue 8. (ISSN 2250 3153) [9]

[18]. Pushpa Raikwal, Vaibhav Neema, Sumant Katiyal, "Low power High speed with improved Noise Margin for Domino CMOS Inverter", Indian Journal of Applied Research, Volume 1, Issue 7, April 2012. (ISSN -2249-555X)[9]

[19]. Vaibhav neema , Pushpa Raikwal, Sumant Katiyal , "Low power High speed with improved Noise Margin for Domino CMOS nand Gate", International Journal of Computational Research, Volume 2, March-APRIL 2012. (ISSN -2250-3005). [9]

[20]. Vaibhav Neema and Sanjiv Tokekar, "Analysis of Dual Threshold Voltage over Low Power design techniques for CMOS digital", Published as a Research Article in Inventi Journal of Engineering and Technology, Volume 2011-Issue 2, April - June 2011, ISSN: 2230–9202.

[21]. Vaibhav Neema, S.S.Chouhan, Sanjiv Tokekar, "Novel Circuit Technique for Reduction of Leakage Current in Series/Parallel PMOS/NMOS Transistors Stack", Paper Published in IETE JOURNAL OF RESEARCH, Vol 56, ISSUE 6, Nov-Dec 2010, pp 362-364. **UGC File III no 58**

[22]. Vaibhav Neema, S.S.Chouhan, Sanjiv Tokekar , "Graph theory based approach for determination of input vectors of CMOS VLSI circuits responsible for leakages ", paper published in International Journal of Electronics & Telecommunication and Instrumentation Engineering, at SERC India, ISSN 0974-4975, IJETIE , January 2010-March 2010, Spring Edition 2010, pp 13-16, Volume 01, issue No 01.

**International/ National Conferences:**

[1]. Priyanka Parihar, Neha Gupta, Vaibhav Neema and Praveen Singh, "Investigation of MTCMOS 6T SRAM cell for ultra-low power application" 2nd International Conference on Nano-electronics, Circuits & Communication Systems (NCCS-2016), Institution of Electronics & Telecommunication Engineers, Ranchi & ISVE Ranchi, 25-26 Dec 2016.

[2]. Neha Gupta, Priyanka Parihar, Vaibhav Neema and Praveen Singh, "Novel approach for Sleep Transistor Sizing to suppress power and ground bouncing noise in MTCMOS clustering Technique" 2nd International Conference on Nano-electronics, Circuits & Communication Systems (NCCS-2016), Institution of Electronics & Telecommunication Engineers, Ranchi & ISVE Ranchi, 25-26 Dec 2016.

[3]. Praveen Singh, Vaibhav Neema, Shreeniwas Daulatabad and Ambika Prasad Shah, "Subthreshold Circuit Designing and Implementation of Finite Field Multiplier for Cryptography Application", **Elsevier Procedia Computer Science**, Vol. 79, 2016, pp. 597- 602. [Impact: 0.705]

[4]. Shreeniwas Daulatabad, Vaibhav Neema, Ambika Prasad Shah and Praveen Singh, "8-Bit 250-MS/s ADC Based on SAR Architecture with Novel Comparator at 70 nm Technology Node", **Elsevier Procedia Computer Science**, Vol. 79, 2016, pp. 589-596. [Impact: 0.705]

[5]. Ambika Prasad Shah, Vaibhav Neema and Shreeniwas Daulatabad, "Comparative study of Area, Delay and Power Dissipation for LECTOR and INDEP (Leakage control techniques) at 70 nm technology node", 2015 IEEE International Advance Computing

Conference (IACC 2015), B.M.S. College of Engineering, Bangalore, 12-13, June 2015, pp. 513-518. (DOI: 10.1109/IADCC.2015.7154761)

[6]. Ambika Prasad Shah, Vaibhav Neema and Shreeniwas Daulatabad, "Effect of Process, Voltage and Temperature (PVT) Variations in LECTOR-B (Leakage control technique) at 70 nm technology node ", 2015 IEEE International Conference on Computer, Communication and Control (IC4 -2015), Medi-Caps Group of institutions, Indore, 10-12, September 2015.

[7]. Ambika Prasad Shah, Vaibhav Neema and Shreeniwas Daulatabad, "A Novel Leakage Reduction DOIND Approach For Nanoscale Domino Logic Circuits"(Extended version of RSC 2015), 2015 IEEE International Conference on Contemporary Computing (IC3 2015), Jaypee Institute of Information Technology, Noida, 20-22, August 2015.

[8]. Ambika Prasad Shah, Vaibhav Neema and Shreeniwas Daulatabad, "PVT Variations Aware Low Leakage DOIND Approach For Nanoscale Domino Logic Circuits", 2015 IEEE Power, Communication and Information Technology Conference (PCITC -2015), Siksha 'O' Anusandhan University, Bhubaneswar "Accepted"

[9]. Ambika Prasad Shah, Vaibhav Neema and Shreeniwas Daulatabad, "Comparative analysis of DOIND Approach With and Without Body Biasing for Leakage Reduction in Domino Logic Circuits", 2015 IEEE International Conference on Signal Processing, Computing and Control (ISPCC 2015), Jaypee university of Information Technology, Waknaghat (H.P.).

[10]. Ambika Prasad Shah, Vaibhav Neema and Shreeniwas Daulatabad, "A Novel Leakage Reduction DOIND Approach For Nanoscale Domino Logic Circuits", Research Scholar Congress 2015, Indian Institute of Technology (IIT) Guwahati, 23-24 May 2015.

[11]. Garima Nayak , Shubham Tiwari, Vaibhav Neema , "Sleep transistor sizing in MTCMOS Circuit for Low Power, Loe Delay circuit designing" in National Conference on Microelectronics , Networking and Communication (NCMNC-2015), SRM University Chennai 30-31 March 2015.

[12]. Abhijeet Singh, Amrisha Singh, Pravesh Sahu and Vaibhav Neema, "Optimization of Power Dissipation in CMOS Circuit utilizing W/L parameter of the Sleep Transistor". In Advance Research in Electrical and Electronics Engineering (AREEE), Volume 2, Number 8, April –June 2015. ISSN 2349-5804, pp37-39.

[13]. Vaibhav Neema , Rajesh Naiyk and Chandan Joshi, "Voltage Scaling Techniques for Low Power Digital VLSI Chips." In ICE-ICEE held in SVITS, Indore (M.P.) on 23 January 2014.

[14]. Pragya Tiwari and Vaibhav Neema, "Performance Evaluation of 6T SRAM cell structure and peripheral circuitry, National Conference on Advance in Electronics and Communication Engineering (AECE) , at SVCE , March 2013.

[15]. Vaibhav Neema, Shivangani Saxena and Namrata Dixit, "One Bit Full Adder For Sub-Threshold Logic Design" Presented in National Conference on Advances in Electrical and Electronics Engineering (AEEE-2011) at SVCE, Indore, during 24-25 Feb, 2011.

[16]. Vaibhav Neema, Shivangani Saxena and Namrata Dixit, "Performance Evaluation and Development of Sub threshold Library Cell Components" Presented in National Conference on Recent Trends in Electronics & Communication Technology (ECOMM-2011) at SD- Bansal , Indore, during 8-9 April , 2011.

[17]. Vaibhav Neema and Mahesh Kumawat, "Low power, High Speed & Large Gainbandwidth three stage Operational amplifier" presented in International conference on Advanced Computing , communication and Networks [ICACCN-11] which will held at Chandigarh on 02-03 june, 2011.

[18]. Vaibhav Neema and Kapil Sahu , "Implementation of WCDMA rake Receiver Used in 3G Wireless Communication using VHDL", Presented in 4th National Conference & ISTE State Chapter Annual Convention on NCWCVD-2011 at Gwalior, MP, during May 29th , 2011.

[19]. Vaibhav Neema , "Ultra Low Power 1-Bit Full Adder for Bio-Medical / Battery Operated VLSI Circuit Designing" Presented in 26th Young Scientist Congress held in JNKVV, Jabalpur during 28th FEB- 1st MARCh -2011.

[20]. Vaibhav Neema and Sanjiv Tokekar, "VSECURE: Active & Standby Subthreshold Leakage Current Reduction Technique" Published in the Proceeding of 22nd IEEE technically co-sponsored International Conference on Microelectronics ICM'10 will be held in Cairo, Egypt. ICM' 10 held in cooperation with the American University in Cairo and the University of Waterloo, IEEE catalog number: CFP10473-CDR, ISBN: 978-1-61284-150-2.

[21]. Vaibhav Neema and Sanjiv Tokekar, "Scaling Effect over Proposed Technique "VSECURE" for Static Power Reduction in Digital CMOS VLSI circuits" Published in Proceeding of NuiCONE-2010 in International Conference on Current Trends in Technology (NUiCONE 2010), Ahmedabad, India

[22]. Vaibhav Neema and Sanjiv Tokekar, "Analysis and Minimization Technique for Leakage Reduction in Two Input NOR gate" published in Proceeding of in International Joint Journal Conference in Engineering, AET 2010 - Trivandrum, Kerala, India ( ISBN 978-81-910691-4-3) pp 160-164.

[23]. Vaibhav Neema, S.S.Chouhan, Sanjiv Tokekar, "Novel Circuit Technique for Reduction of Active Drain Current in Series/Parallel PMOS Transistors Stack", published in proceedings of 2010 International Conference on Electronic Devices, Systems & Applications at Universiti Teknologi MARA, Malaysia, 11th April -14th April 2010. IEEE Xplore database and Indexed in Scopus IEEE Catalog Number: CFP1057J-ART(ISBN: 978-1-4244-6632-0).

[24]. Vaibhav Neema, S.S.Chouhan, Sanjiv Tokekar , "Novel Circuit Technique for Reduction of Active Drain Current in Low Leakage Digital VLSI Circuits", published in Proceedings of ICWET-2010, Mumbai, research paper is also uploaded by ACM Digital Library and available at http://portal.acm.org

[25]. Vaibhav Neema, S.S.Chouhan, Sanjiv Tokekar, "computation of Various Leakage currents in CMOS based 2 input NAND gate using SCS model" Proc of International Conference on Recent Advancement in Electrical Science( ICRAES'10), 8th – 9th Jan, 2009.

[26]. Vaibhav Neema, S.S.Chouhan , Praveen Singh , "Comparative Study of NAND and NOR gate for Low Power High Speed Nanoscale CMOS Circuit" IEEE Proc of International Conference (CICSyN, 2009), 23-25 July 2009, Indore, India.

[27]. Vaibhav Neema, S.S.Chouhan, "Realization of two input AND gate using Domino CMOS logic" ETET-2009 at SVCE, Indore, India.

[28]. Vaibhav Neema, Dr. Sanjiv Tokekar, "Dynamic Voltage Scaling for Designing of Low Power Microprocessor", NCAFIS, 08 at DAVV, Indore (MP), India.

[29]. Vaibhav Neema, Dr. Sankar Sarkar, "Crosstalk between VLSI Interconnects" Proc. Of National Conference, "DTVC-2007" at NIT, Hamirpur HP, India.

[30]. Pradeep Kumar, Vaibhav Neema, Nidhi Gupta, "Fractional Hartley Transform-A Review", Proc. of national conference, BBSEC, Fatehgarh Sahib-India.

[31]. Pradeep Kumar, Vaibhav Neema, Kulbir Singh, "Comparative Study of Discrete Cosine and Fourier Transform in Image Compression", Proc. Of International conference, Engineering College, Bikaner-India.

[32]. Pradeep Kumar, Vaibhav Neema, A. P. Rao, "Comparative Study of Discrete Fourier and Hartley Transform in Image Compression" Proc. Of National conference ETA-2005, Rajkot-India.

[33]. Vaibhav Neema, Santosh Vishwakarma , "Advantages and Challenges of GaAs Technology" Proc of IMS conference-04, Chandigarh, India. (http://www.imsindia.org.in/)

[34]. S. K. Vishvakarma and Vaibhav Neema, "Delta Sigma Analog to Digital Converter", Indian Microelectronics Society (IMS) Conference, Chandigarh, India, 18th -20th, Feb., 2005. For detail click here (http://www.ims-india.org.in/).

## ➢ Award:

- ✓ Received **50% Travel Grant** from **MPCST** for attending International Conference on Electronic Devices, Systems & Applications (ICEDSA-2010) organized by Centre for Electronic Engineering Studies, Faculty of Electrical Engineering, Universiti Teknologi MARA, **Malaysia,** 12th April -14th April 2010.
- ✓ Best Paper award in the category **Advances in Electrical Engineering**, International Joint Conference on Advances in Engineering and Technology (AET-2010), Trivandram, Kerala, India, 21st-22nd Dec, 2010.
- ✓ Certificate of Appreciation for Best Paper award by students at International Conference on Science and Innovation Engineering 2015, Chennai on 5th April 2015.
- ✓ Recipient of Scholarship for securing 3rd rank in Devi Ahilya University, Indore in Master of Science Year 1999.

## ➢ Professional Activities:

- ✓ VLSI, IEEE Computer Society Technical Committee Member: 90305198.
- ✓ Member of IEEE Transactions on Evolutionary Computation.
- ✓ Senior Member , Universal Association of Computer & Electronics Engineering (UACEE): SNM1004637

- ✓ International Association of Computer Science and Information Technology (IACSIT) Member : 80338451
- ✓ International Journal of Engineering Research (IJER) reviewer member :
- ✓ Editorial & Reviewer board member for International Journal of Computer and Electrical Engineering (IJCEE)
- ✓ Review Member of Journal of Nanotechnology and Optoelectronics Journal recognized by UGC**.**

➢ **Paper Reviewer:** Review Member:

- ✓ IEEE International Conference on Computer Communication and Control organized by MediCaps Institute, Indore, 10-11 Sep 2015.
- ✓ ADINA Young Scientist Award 2016, Organized by ADINA Group of Institute, Sagar, 5th March 2016.
- ✓ **National Conference organized by School of Electronics**, Devi Ahilya University, Indore (MP) during 2 &3 April, 2010
- ✓ **VDAT 2010 - 14th IEEE/VSI VLSI Design and Test Symposium**, July 7-9, 2010 at Chitkara Institute of Engineering & Technology Chandigarh.
- ✓ **The International Conference on Communication Systems and Network Technologies 2011**, Mata Vaishno Devi University, Katra Jammu, India, during 3-5 Jun 2011.
- ✓ **The International Conference on Computational Intelligence and Communication Networks (CICN2011),** Gwalior (MP), During **7**-9 Oct 2011.
- ✓ Reviewer Member for National Conference on "Recent Trends in Engineering and Science (NCRTES-2012) Organized by Prestige Institute of Engg & Science, Indore during 20-21 April 202.
- ✓ Review member for IEEE Transactions on Circuits and Systems II, CAS-II

➢ **Invited Talk / courses and Session Chair**

- ✓ Delivered Lightning Talk on IoT Enabled smart Education System, 5th International Conference on Advance in Computing, Communication and Informatics, Jaipur, 21-24 Sep 2016.
- ✓ National Conference on Contemporary Computing, Organized by CITM, Indore, 21-22 Oct, 2016.
- ✓ National Conference Organized by Indore Institute of Science and Technology during 17th-18th April, 2010.
- ✓ Chaired technical session in 2010 International Conference on Electronic Devices, Systems & Applications (ICEDSA-2010) held at the Best Western Seri Pacific Hotel in **Kuala Lumpur, Malaysia** during 12-14 April, 2010.
- ✓ Technical Talk on "issues related to Low power VLSI Circuit Design" at Indore Institute of Science and Technology.
- ✓ 2 Days Technical Session organized by veserve Global institution on "VLSI Design and application".

- ✓ International Institute of Professional Studies (IIPS-D.A.V.V.) invite to taught a course on VLSI Design for MCA XI th Semester Students
- ✓ School of Electronics, D.A.V.V. invited to taught a course on CMOS Digital design for M.Sc (Electronics) students.
- ✓ School of Instrumentation, D.A.V.V. invited to taught course on VLSI Technology for M.Tech students.

➢ **Workshop attended/ organized:**

- ✓ Attended Industry Academia Conclave organized by IIT-Indore, 18-20 Feb 2016.
- ✓ Attended three days Faculty Development Program on Smart System, Organized by IET-DAVV, Indore, 8-10 Dec 2016.
- ✓ Attended One Week workshop on Modeling , Simulation and Characterization of Nano-Transistor, organized by IIT Kanpur during October , $26^{th}$- $30^{th}$ , 2015.
- ✓ Attended two days workshop on "Capacity Building Programme on Bio-Medical and E Waste Management" **organized by International Institute of Waste Management (IIWM), Bhopal during 27-28 July, 2015.**
- ✓ Organized two week ISTE workshop on "Control Systems" from $2^{nd}$ Dec 2014 to $12^{th}$ Dec 2014.
- ✓ Attended one week ISTE workshop on "Control Systems" **Indian Institute of Technology, Kharagpur (IIT-KGP) from $15^{th}$ Sep -$19^{th}$ Sep, 2014.**
- ✓ Attended one week ISTE workshop on Signals and Systems" **Indian Institute of Technology, Kharagpur (IIT-KGP) from $2^{nd}$ Dec-$12^{th}$ Dec, 2013.**
- ✓ Organized two week ISTE workshop on "Analog Electronics" from $4^{th}$ June 2013 to $14^{th}$ June 2013.
- ✓ Organized two days workshop on "Next Generation Networks" from $27^{th}$ -$28^{th}$ Jan 2012.
- ✓ Attended one week ISTE Coordinator workshop on "Analog Electronics " **Indian Institute of Technology, Kharagpur (IIT-KGP) during $1^{st}$ April – $5^{th}$ April 2013**
- ✓ Member of University Industry partnership cell at Devi Ahilya University , Indore
- ✓ Attended Fifth SERC School on "New Developments in Microfabrication with Focus on Synchrotron Radiation based Deep X-ray Lithography" **Raja Ramanna Centre for Advanced Technology (RRCAT), Indore during October 29-November 03, 2012**
- ✓ Attended Two week ISTE Workshop for **Basic Electronics** under the national mission on education through ICT conducted by **IIT Bombay at SGSITS, Indore**, during $28^{th}$ June to $8^{th}$ July 2011.
- ✓ Participated in Faculty Development Programme on **Wireless Computing, Green Computing** held on 26 August 2010 at IET-DAVV Indore conducted by **Tata Consultancy Services (TCS).**
- ✓ Attended Two Days $2^{Nd}$ INUP Workshop on **"Nanofabrication Technologies"** at IIT Mumbai

- ✓ **Organizing Member** & Attended Three days National workshop on **"Recent Trends in Microelectronics and VLSI -07",**at SGSITS, Indore(MP)
- ✓ Attended Three days National workshop on **"Recent Trends in NANO-TECHNOLOGY-07"** organized by SGSITS, Indore.
- ✓ Participated Three days National workshop on "**VLSI design and Embedded System"** organized by BITS Pilani (Raj), 2006.
- ✓ Attended Three Days International Conference On **"Physics for World"** organized by Engineering College, Bikaner (Raj), 2005.
- ✓ Attended Three Days National Conference organized by BBSBE, Fatehegarh Sahib Punjab, 2005.
- ✓ Attended Three Days National Conference On **"Emerging Technology and Application"** organized by saurashtra University, Rajkot (Guj), 2005.
- ✓ Attended Four Days International radar Symposium organized by **IISc**, Bangalore, 2005.
- ✓ Participated Three days IMS National conference organized SCL, CSIO and Panjab University, Chandigarh, 2005.

➢ **Professional Achievements:**

- ✓ Member of Selection Committee Meeting for Recruitment of Asstt. Professor, at SGSITS, Indore, 02 Jun 2016.
- ✓ Exam Committee member for Session April – Amy 2017, for Theory and Practical Exam Panel at IET DAVV, Indore.
- ✓ External Member of Board of Studies (BOS) for Faculty of Electronics & Communication Engg, Dr A.P.J. Abdul Kalam University, Indore, (MP).
- ✓ Committee member for developing proposal for University with Potential of Excellence for Devi Ahilya University , Indore
- ✓ Task Group Member of University Profiling and Development proposal at Devi Ahilya University , Indore (we as member prepare proposals for Thomson reuters, University for Potential of Excellence, Modern University)
- ✓ Assistant superintendent of exam for session Nov-Dec, 2015 at IET-DAVV, Indore.
- ✓ Officer on Special Duty (OSD) for Revaluation and Review work at IET-DAVV, Indore for session Jan-March, 2015.
- ✓ Committee member for Choice Based Credit System (CBCS) Scheme at IET-DAVV, Indore.
- ✓ Officer on Special Duty (OSD) for Central Valuation work at IET-DAVV, Indore for Session Nov-Dec, 2014.
- ✓ Officer on Special Duty (OSD) for Revaluation and Review work at IET-DAVV, Indore for session Jan-March, 2014.
- ✓ Assistant superintendent of exam for session April-May, 2013 at IET-DAVV, Indore.

- ✓ Officer on Special Duty (OSD) for Revaluation and Review work at IET-DAVV, Indore for session Jan-March, 2013.
- ✓ Assistant superintendent of exam for session April-May, 2011 at IET-DAVV, Indore.
- ✓ Committee member of Theory/ practical examination examiner panel for Nov-Dec, 2010.
- ✓ Departmental Committee member for TEOIP World Bank project 2010.
- ✓ Officer on Special Duty (OSD) for Central Valuation work at IET-DAVV , Indore for Session May-Jun, 2010.
- ✓ Developed Curriculum for VLSI subjects for UG and PG Courses in IET-DAVV, Indore
- ✓ Assistant superintendent of exam session Nov-Dec, 2008 at IET-DAVV, Indore.
- ✓ Establishing VLSI Design Lab for UG and PG programme at IET-DAVV, Indore
- ✓ Visiting Faculty for VLSI subjects in UTDs of Devi Ahilya University , Indore
- ✓ Time table incharge for E&TC and E&I department for Session Jun-Dec, 2009 in IET –DAVV, Indore.
- ✓ Developed VLSI design lab to start M.Tech. Program specialization in VLSI design at MITS, Lakshmangarh Sikar (Raj) under guidance of Dr Sankar Sarkar (retd. Professor IIT Roorkee) Dean Faculty of Engineering, MITS, Lakshmangarh.
- ✓ Member of admission committee board for M.Tech VLSI design at MITS, Lakshmangarh.
- ✓ Lab incharge for M. Tech VLSI Design Lab at MITS, Lakshmangarh.
- ✓ Honored by best faculty according to the student feed back at MITS Lakshmangarh.
- ✓ Introduces Teacher- Guardian scheme in the Institute and worked as coordinator of the scheme at COER, Rookee.
- ✓ Awarded by Telescopic award for achieving the 100% results by COER, Roorkee.
- ✓ Member of technical committee in COER, Roorkee during July 03 to Jun 04.
- ✓ Developed CAD Lab for B.Tech Programme at COER, Roorkee.
- ✓ Lab & Time Table in-charge for Electronics Department of COER, Roorke during July 04 to Dec 05.

Dr Vaibhav Neema

Indore